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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,959	06/20/2001	Hidemasa Zama	210067US-2	2668

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
TAN, VIBOL

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,959	ZAMA ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,5-13 and 15-17* is/are allowed.

6)☒ Claim(s) *3,4 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 3, 4, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwaki et al. (U. S. PAT. 6,208,170).

Iwaki et al. teaches all claimed features of claims 3 and 4 in Fig. 3, a logic operation circuit comprising: two or more gate circuits (col. 3, line 49; 102 having plurality of low threshold voltage transistors to constitute a functional logic circuit), each being connected between a virtual voltage line (QVCC) and a first reference voltage line (VSS) and constituted by a plurality of first transistors (col. 3, line 50; 102 have a lower threshold); a control circuit (clock circuit used to control transistor 104, not shown) configured to control the operation of said two or more gate circuits; and a second transistor (104) which is connected between a second reference voltage line (VCC) and said virtual voltage line and constituted by a transistor (col. 4, line 28) having a threshold voltage higher than that of each of said first transistors (transistors inside 102), a source/drain terminal of each of said first transistors in said gate circuit being connected to either a source/drain terminal of another first transistor in said gate circuit

(similar manner to the connections inside 301 in Fig. 4 depends on desired logic functions) or an output terminal (output from 102) of said gate circuit, wherein said logic operation circuit is provided on a critical path (operates at a high speed; col. 3, line 51).

In claim 14, Iwaki et al. teaches in Figs. 3 and 4, a Flip flop comprising: a first conduction interception circuit (101) capable of switching conduction or shutoff (in response to the logic states of 104 and 105) between an input terminal (→, input for 101) and an output terminal (→, output for 101); a first storage (103) circuit capable of holding output logic of said first conduction interception circuit (101); a second conduction interception circuit (102) which is capable of switching conduction or shutoff (in response to the logic state of 104) between an input terminal (input for 102) and an output terminal (output for 102), and has said input terminal being connected to an output terminal of said first storage circuit; and a second storage circuit (shown by dashed lines, would be another storage circuit after 102) capable of holding output logic of said second conduction interception circuit (holds the output of 102), said first and second conduction interception circuits each including: two or more gate circuits (col. 3, line 49; 102 having plurality of low threshold voltage transistors to constitute a functional logic circuit), each being connected between a virtual voltage line (QVCC) and a first reference voltage line (VSS) and constituted by a plurality of first transistors (col. 3, line 50; 102 have a lower threshold); a control circuit (clock circuit used to control transistor 104, not shown) configured to control the operation of said two or more gate circuits; and a second transistor (104) which is connected between a second reference voltage line (VCC) and said virtual voltage line and constituted by a transistor (col. 4, line 28)

having a threshold voltage higher than that of each of said first transistors (transistors inside 102), a source/drain terminal of each of said first transistors in said gate circuit being connected to either a source/drain terminal of another first transistor in said gate circuit (similar manner to the connections inside 301 in Fig. 4 depends on desired logic functions) or an output terminal (output from 102) of said gate circuit, wherein said logic operation circuit is provided on a critical path (operates at a high speed; col. 3, line 51).

3. Claims 1, 5-13, and 15-17 appear to comprise allowable subject matters.

Response to Arguments

4. Applicants arguments filed 7/17/2003 have been fully considered but they are not persuasive. Applicants have not overcome the prior art rejection under 35 U.S.C. 102(e) as being anticipated by Iwaki et al. Iwaki et al. anticipates all claimed limitations of the amended claims 3, 4, and 14, as explained in details above.

5. The rejection of claims 3, 4, and 14, is maintained.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (703) 306-5948. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (703) 305-3493. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0959.

Vibol Tan

Patent Examiner, AU 2819